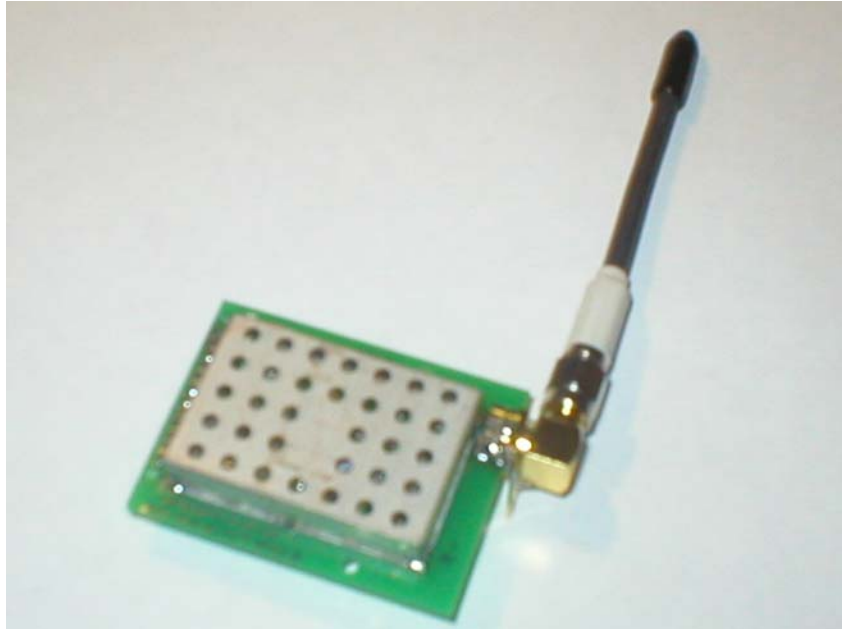


R900 Preliminary Specification

R900 is a full transceiver radio module operates in the 900Mhz ISM band radio. Requires no license to operate it. It uses FSk modulation to support up to 1.5 Mbs with 20dbm output power and -95dbm receive sensitivity. It supports up to 50 channels at 512Khz spacing with 1Mhz channels facilitating Frequency hopping to be easily implemented.



It requires three wires for configuration interface (clk, En and Data) and requires two data lines (RX and TX). It also requires a reference frequency of 6.144 or 12.288 Mhz and radio enable (XCEN) as well as line to switch between RX and TX (RXON). The radio is designed for ease of interface to the users system to help reduce the wireless system design cycle and enable an earlier product introduction to the market.

Features

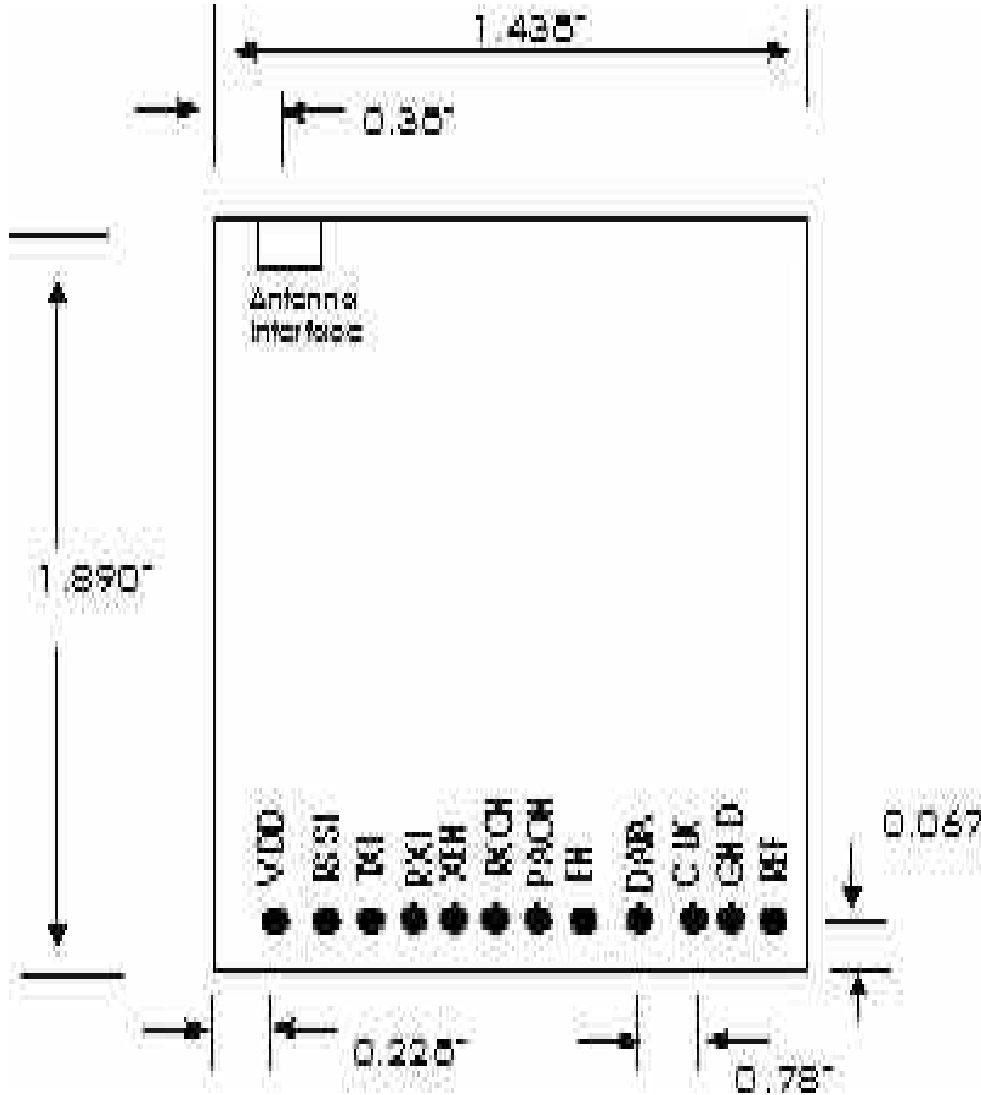
- Complete 900MHz FSK Transceiver
- High data rate (1.5Mbps)
- -95dBm sensitivity.
- 20dBm Output Power (differential, typical)
- Low IF Receiver: No external IF filters required.
- Fully Integrated frequency synthesizer:
- No external resonator required.
- Automatic Filter Alignment
- No manufacturing adjustments required.
- No external data slicer components required
- 3-wire control interface
- Analog RSSI output

Applications

- Digital Cordless Telephones
- Wireless PC Peripherals
- Wireless Game Controllers

- Wireless Streaming Media

Mechanical Dimensions



Specifications

	Min	Typ.	Max	Units
Operating Temp.	-10		50	C
Output Power		+20		dbm
Input Sensitivity		-95		dbm
VDD	2.7		3.8	V
I _{VDD TX}		55	300	ma
I _{VDD RX}		55	76	ma
StandBy Current		10	120	ua

Rxon to valid Data		70	120	usec
XCEN high to valid RX Data (XCEN low period >120usec)		320	342	usec
Lock for channel switch		420	342	usec
F _{ref}		6.144 12.288		Mhz Mhz
RSSI max. Range	1.4	1.8	2.3	V
RSSI Sensitivity	28	38	42	Mv/db
V _{IHI}	Never exceed VDD	075*VDD	VDD	V
V _{I Low}	0		0.25*VDD	V
V _{OHI}	VDD-0.4			V @ 0.1ma
V _{O Low}			0.4	V @ -0.1ma

Pin Description

VDD	I	Power Connection
RSSI	O	Buffered Analog output nominal sensitivity 35mv/db
TXI	I	Data Transmit
RXI	O	Data receive
XCEN	I	When set to 1 radio enabled, when set to 0 the radio in standby mode.
RXON	I	When set to 1 the radio is in RX mode, When set to 0 the radio in the TX mode.
PAON	O	External PA control
EN	I	Enable writing to the internal configuration registers
Data	I	Data line for writing to the internal registers. The least two bits are used as an address to select between the three internal registers.
CLK	I	Clock used to latch the date at the internal registers.
GND	I	Reference voltage to the radio.
Fref	I	6.144 or 12.288 reference frequency for the radio

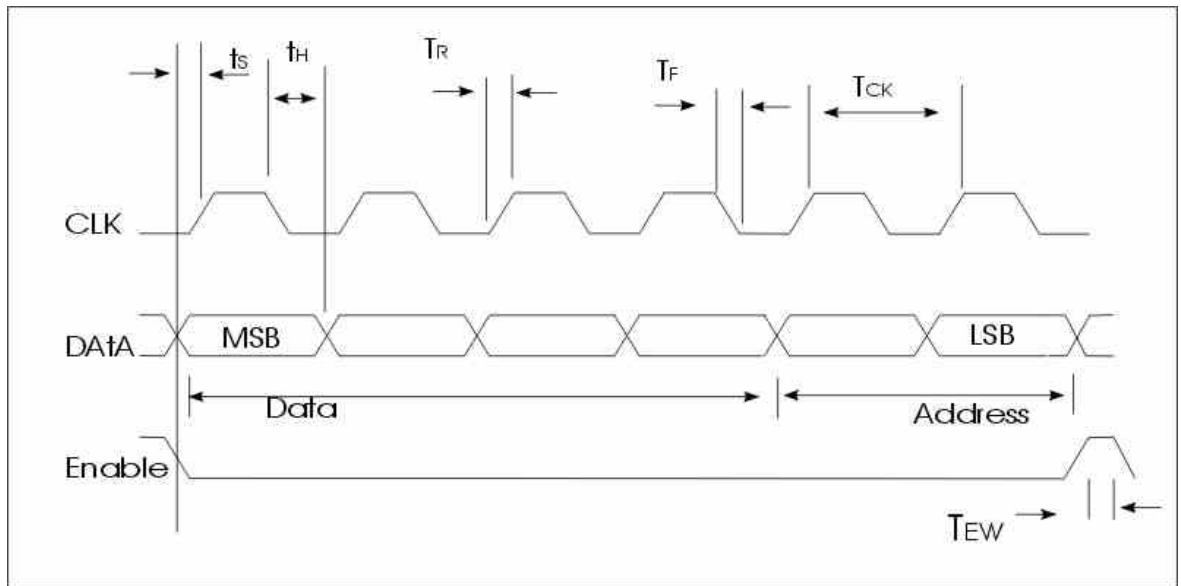
The three Wire interface

Three wires are required to enable to write to the three configuration registers

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
BUS CLOCK (CLK)					
tr	CLK input			15	Ns

	rise time				
tf	CLK input fall time			15	Ns
tck	CLK period	50			Ns
ENABLE (EN)					
tew	Minimum pulse width	100			Ns
tl	Delay from last CLK rising edge	15			Ns
tse	Set up time to ignore next rising CLK	15			Ns
BUS DATA (DATA)					
ts	Data to clock set up time	15			Ns
th	Data to clock hold time	15			Ns

3-Wire Bus Timing Characteristics



Configuration Registers

Register 0 -- PLL Configuration Register

Bit	NAME	DESCRIPTION	DEFINITION
15	Reserved	Reserved	Set to 0
14	Reserved	Reserved	Set to 0
13	Reserved	Reserved	Set to 0
12	Reserved	Reserved	Set to 0
11	Reserved	Reserved	Set to 0
10	Reserved	Reserved	Set to 0
9	Reserved	Reserved	Set to 0
8	Reserved	Reserved	Set to 0
7	TPC	Transmit Power Control	0: AOUT pin pulled to ground 1: AOUT pin high impedance
6	TXCL	Transmit Test Mode	0: FSK modulation in Transmit mode 1: CW (no modulation in Transmit mode)
5	LOL	PLL Frequency Shift 0: LO shift is 0 Hz for Transmit	1.024 MHz for Receive
4	RXCL	PLL Mode in Normal Receive Operation	0: PLL open loop during Receive 1: PLL closed loop during Receive
3	RD0	Reference Frequency Select	0: 6.144MHz nominal reference frequency 1: 12.288MHz nominal reference frequency (preferred)
2	QPP	PLL Charge Pump Polarity	0: For $f_c < f_{ref}$, charge pump sources current 1: For $f_c < f_{ref}$, charge pump sinks current
1	ADR1	MSB Address Bit	ADR1=0
0	ADR0	LSB Address Bit	ADR0=0

Register 1 -- Channel Frequency Register

Bit	NAME	DESCRIPTION	DEFINITION
15	Reserved	Reserved	Set to 0
14	Reserved	Reserved	Set to 0
13	CHQ11	Channel frequency Select bits	Divide ratio= $f_c/1.024$
12	CHQ10	Channel frequency Select bits	Divide ratio= $f_c/1.024$
11	CHQ9	Channel frequency Select bits	Divide ratio= $f_c/1.024$
10	CHQ8	Channel frequency Select bits	Divide ratio= $f_c/1.024$
9	CHQ7	Channel frequency Select bits	Divide ratio= $f_c/1.024$
8	CHQ6	Channel frequency Select bits	Divide ratio= $f_c/1.024$

7	CHQ5	Channel frequency Select bits	Divide ratio=fc/1.024
6	CHQ4	Channel frequency Select bits	Divide ratio=fc/1.024
5	CHQ3	Channel frequency Select bits	Divide ratio=fc/1.024
4	CHQ2	Channel frequency Select bits	Divide ratio=fc/1.024
3	CHQ1	Channel frequency Select bits	Divide ratio=fc/1.024
2	CHQ0	Channel frequency Select bits	Divide ratio=fc/1.024
1	ADR1	MSB Address Bit	ADR1=0
0	ADR0	LSB Address Bit	ADR0=1

$$F_c = 1.024 * CHQ \text{ Mhz}$$

: Register 2 – Test Mode Register

Bit			
15	Reserved	Reserved	Set to 0
14	Reserved	Reserved	Set to 0
13	Reserved	Reserved	Set to 0
12	Reserved	Reserved	Set to 0
11	Reserved	Reserved	Set to 0
10	Reserved	Reserved	Set to 0
9	Reserved	Reserved	Set to 0
8	Reserved	Reserved	Set to 0
7	DTM2	Digital Test Control Bits	
6	DTM1	Digital Test Control Bits	
5	DTM0	Digital Test Control Bits	
4	ATM2	Analog Test Control Bits	
3	ATM1	Analog Test Control Bits	
2	ATM0	Analog Test Control Bits	
1	ADR1	MSB Address Bit	ADR1=1
0	ADR0	LSB Address Bit	ADR0=0

Analog and Digital test mode are used for testing and debugging modes. The following are description of each state.

Analog Test Table

ATM2	ATM1	ATM0	RSSI	TPC/TPQ (internal node to the radio)
0	0	0	RSSI	Set by AOUT bit
0	1	0	I IF Filter Output	Q IF Filter Output
0	1	0	I IF Filter Output	Q IF Filter Output
0	1	1	Q IF Filter – ve Output	Q IF Filter + ve Output

1	0	0	I IF Filter – ve Output	I IF Filter + ve Output
1	0	1	Data Filter + ve Output	Data Filter – ve Output
1	1	0	I IF Limiter Outputs	Q IF Limiter Outputs
1	1	1	1.67V Voltage Reference VCO	Modulation Port Input

Digital Test Table

DTM2	DTM1	DTM0	RX
0	0	0	Data Out
0	0	1	AGC Switch State
0	1	0	PLL Main Divider Output
0	1	1	PLL Reference Divider Output